CLAIMS

1. (Original) A data processor for use in a wireless communication device, comprising:

a processing unit;

an instruction pipeline circuit;

at least one processing module;

a timer for generating a time-out interval; and

power control logic for detecting a sleep instruction and placing the processing unit, instruction pipeline circuit and at least one processing module in a low-power state, where the power control logic is operative in response to a wake-up signal to reactivate the instruction pipeline circuit, and consequently at least one processing module only to the extent required by the wake-up signal.

2. (Original) The processor of claim 1, where the instruction pipeline circuit comprises a multi-stage instruction pipeline circuit.

3. (Original) The processor of claim 1, where the wake-up signal comprises a logical OR combination of one or more predetermined wake-up conditions and the time-out interval.

4. (Original) The processor of claim 1, where the power control logic comprises instruction decode logic to detect the sleep instruction.

5. (Original) The processor of claim 1, where the power control logic comprises branch condition logic to respond to the wake-up signal.

6. (Original) The processor of claim 1, where the power control logic, having specified one or more wake-up conditions that the processing unit will respond to when in a low-power state, generates the wake-up signal upon detecting the one or more wake-up conditions or the time-out interval.

7. (Original) The processor of claim 1, where the power control logic instructs the instruction pipeline circuit to complete any instructions preceding the sleep instruction.

8. (Original) The processor of claim 7, where the power control logic instructs the instruction pipeline circuit to cease fetching new instructions after encountering a sleep instruction whose wake-up conditions are currently deasserted.

9. (Original) The processor of claim 1, wherein the processing unit, instruction pipeline circuit and at least one processing module are formed together on a common silicon substrate using CMOS processing.

10. (Original) The processor of claim 6, wherein the wake-up conditions and time-out interval are stored in a register by the power control logic.

11. (Original) An article of manufacture having at least one recordable medium having stored thereon executable instructions and data which, when executed by at least one processing device, cause the at least one processing device to:

detect a sleep instruction for the processing device;

specify one or more wake-up conditions and a time-out interval;

power down an instruction pipeline and one or more processor modules;

reactivate the instruction pipeline upon detection of a wake-up signal corresponding to either a wake-up condition or the time-out interval, and

process one or more instructions in the instruction pipeline to reactivate any of the one or more processor modules required to respond to a detected wake-up condition.

12. (Original) The article of manufacture of claim 11, wherein the processing device executes any instructions received by the instruction pipeline before the sleep instruction is received.

13. (Original) The article of manufacture of claim 11, wherein the instruction pipeline comprises a multistage instruction pipeline, and the processing device reactivates only

stages in the multistage instruction pipeline and/or the function units needed to process one or more instructions necessary to analyze and respond to the wake-up signal.

14. (Original) The article of manufacture of claim 11, further comprising a register for holding the specified wake-up conditions and time out signal.

15. (Original) The article of manufacture of claim 11, where the processing device is implemented as part of a single-chip wireless communication device.

16. (Original) The article of manufacture of claim 11, where the executable instructions and data comprise control logic for controlling the operation of the processing device.

17. (Original) The article of manufacture of claim 11, where the processing device powers down the one or more processor modules by freezing a clock signal for said one or more modules.

18. (Original) The article of manufacture of claim 11, where the processing device powers down the one or more processor modules by placing said one or more modules in an idle mode.

19. (Original) A method for managing power in a communications processor by selectively removing one or more processor modules from a standby mode, comprising:

storing one or more wake-up conditions and a time-out interval in a register;

receiving a processor sleep instruction;

executing any pending instructions received by the processor before the sleep instruction;

powering down the one or more processor modules;

receiving a processor wake-up signal corresponding to one of said wake-up conditions or said time-out interval;

powering up only the processor modules required to respond to the detected processor wake-up signal.

20. (Original) The method of claim 19, wherein one of the processor modules comprises an instruction pipeline circuit.